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Paper Abstract

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Govt. Agency/Lab The Subject Technology Was Developed By/For: **NASA Jet Propulsion Laboratory Contract No. NAS7-1 200**

Category: **Electronics**

Paper 1 itle: **Spacecraft Onboard Information Extraction Computer (SO BIEC)**

Description:

This paper discusses an extremely low power/weight/volume computer node designed for use in spaceborne massively parallel computers. Alternative applications include avionics, embedded computers, portable computing, work station accelerators, and general purpose processing.

INTRODUCTION: SOBIEC integrates a general purpose computer comprising a 32/64 bit microprocessor, up to 16 MBytes of memory, and 14 hi-directional I/O channels into a package roughly equivalent in size, weight, and power dissipation to that of a single chip processor. The resulting computer node is the building block for a massively parallel processor, for a distributed processing system, or a stand-alone embedded processor. The development program is slated for completion in 04 of '93 under a NASA JPL F'base 2 SBIR.

ARCHITECTURAL CONCEPT: SOBIEC couples 3D IC stacking technology with state of the art processor IC technology. The node contains sufficient network 1/0 to implement up to an order-13 hypercube, or any subset thereof. Distributed networks are supported through the same I/O structure, The node has sufficient memory for most multi-computer applications, but also supports external memory expansion and DMA interfaces. Node insertion creates a "smart subsystem" interfaceable to other subsystems via the node's network I/O. Finally, the extreme density offered by this approach makes it an ideal candidate for portable or wearable computing systems. Commercial applications include work station accelerators, data base processors, and massively parallel super computers.

PROCESSOR: I-he nCUBE n2S single chip processor integrates a 64 bit internal/32 bit external data path, floating point unit, memory management, DRAM controller, and 14 hi-directional high speed serial I/O channels. Processor features for high reliability applications include a single error correct/double error detect (SECDED) memory interface and CMOS on epi construction for SEU and latch-up immunity. Throughput is 15 MIPs and 5.1 MFLOPS at 25MHz. Clock rates down to several kHz, software controlled system (re)configuration/partitioning for power management, fault tolerance, degraded mode operation and multi-mission/muhi-mode operation are supported, The addition of 10 DRAM memory ICS completes the computer node,

OPERATING SYSTEM (OS) and SOFTWARE SUPPORT: The nCUBE OS provides configuration and operational support for up to 8000 processors in an order-13 hypercube or any subset or partition(s) thereof. The OS is UNIX (USL SVR4) compatible, C, C+- +, and FORTRAN compilers are available. System stand alone and host-slaved modes are supported.

3-D STACKED MEMORY: Stacking the memories and integrating the stack into the processor package, minimizes size/weight/power and enhances performance and reliability.

SYSTEM CHARACTERISTICS: Package size is 0,72 cubic inches. Average power is 4 Watts with a worst case dissipation of 6 Watts, 32 nodes can be mounted onto a single SEM-E board, though 16 may be a more reasonable number for standard systems without fluid based thermal management.